PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of

Kazuyuki KUWADA, et al.

Docket No: Q79277

Appln. No.: 10/752,700

Group Art Unit: 2891

Confirmation No.: 5921

Examiner: Dana Farahani

Filed: January 8, 2004

For: SEMICONDUCTOR DEVICE AND PROCESS FOR PRODUCING SEMICONDUCTOR DEVICE

APPEAL BRIEF UNDER 37 C.F.R. § 41.37

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. § 41.37, Appellant submits the following:

Table of Contents

I. REAL PARTY IN INTEREST

The real party in interest is Nitto Denko Corporation.

II. RELATED APPEALS AND INTERFERENCES

Appellants, Appellants' legal representative and the Assignee of this application are not aware of any other appeals or interferences that will directly affect, or be affected by, or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-7 are pending in the application. Of these, claims 3-5[1] are withdrawn from consideration.

This is an appeal from the Examiner's rejection of claims 1, 2 and 6 under 35 U.S.C. § 102 and the Examiner's rejection of claim 7 under 35 U.S.C. § 103.

[1] It has been established on the record that claim 2 is a linking claim and is being examined in accordance with MPEP § 809.03. Rejoinder of process claims including claims 3-5 has been requested upon allowance of product claims 1 and 6-7 and/or linking claim 2. See page 5 of the Amendment filed July 25, 2006 and the Statement of Substance of Interview filed July 25, 2006.

IV. STATUS OF AMENDMENTS

The Amendment submitted on July 25, 2006 is the last response submitted with amendments to the claims of the application. The Amendment filed on July 25, 2006 was entered. There are no outstanding amendments to the claims or to the specification in the present application.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

The present invention relates to a semiconductor device and a process for producing the same. Specification, page 1, lines 5-6.

For the purpose of attaining further performance improvements in semiconductor devices, the techniques for connecting a semiconductor element (hereinafter referred to also as "chip") to a lead frame are recently shifting from the wire bonding method, in which gold wires are used for the connection, to wire-less bonding methods in which no wires are used. Typical examples thereof include the flip chip method in which a semiconductor element having bumps formed on the circuit-bearing side thereof is connected facedown to a substrate, e.g., a mother board, which has a wiring circuit formed. Specification, page 1, lines 8-18.

In the flip chip method, a technique is frequently employed in which a liquid resin or sheet-form resin is usually used as an underfill material between the circuit-bearing side of the chip and the substrate and the chip bonding part is sealed with the underfill material. However, for protecting the back (non-circuit side) and the edges of the chip, for example, a method in which these chip surfaces are coated with a liquid resin or covered by over-molding by transfer molding is used. Specification, page 1, line 19 to page 2, line 2.

However, the method in which chip surfaces are coated with a liquid resin has a problem that the corner edge parts of the chip back are apt to be incompletely coated and remain exposed. Specification , page 2, lines 5-8.

On the other hand, the transfer molding method has a problem in that it necessitates a complicated large-scale apparatus for heating and melting a resin, injecting the melt into a mold, and molding and curing it in a high-temperature highly pressurized state and, hence, the selection of conditions is troublesome. Specification, page 2, lines 9-14.

The semiconductor device including a flip chip mounted by face down bonding has an advantage in that the thickness of the semiconductor device itself can be reduced. However, the back and the edges of the chip cannot be effectively sealed by the encapsulation method using a liquid resin. Specification, page 2, lines 15-20.

In particular, in semiconductor devices having two or more stacked layers of the flip chip, there is a problem that semiconductor elements disposed close to each other need to be insulated from each other while attaining a thickness reduction in the semiconductor devices. Specification, page 2, lines 21-26.

Accordingly, an object of the invention is to encapsulate a semiconductor element without fail and to simplify the encapsulation step. In order to eliminate the problems described above, the invention provides a semiconductor device which comprises a substrate and a semiconductor element mounted thereon through a bump bonding part, wherein the semiconductor element has been encapsulated by coating the back and the edges of the semiconductor element with a thermosetting sheet material having tackiness. Specification, page 3, lines 1-10.

Since the back and the edges of the semiconductor element have been coated with a sheet material, the semiconductor element has a satisfactory encapsulated state. This semiconductor device hence has high reliability. Specification, page 3, lines 1-10.

The invention further provides a process for producing a semiconductor device which comprises encapsulating a semiconductor element mounted on a substrate through a bump bonding part, wherein the semiconductor element is encapsulated by coating the back and the edges of the semiconductor element with a thermosetting sheet material having tackiness. Specification, page 3, lines 16-22.

According to this process for semiconductor device production, steps for semiconductor device production can be simplified because the sheet material can be more easily handled than liquid resins and this process is free from the troublesomeness of selection of conditions as in over-molding. Specification, page 3, line 23 to page 4, line 2.

In the process for semiconductor device production of the invention, the tackiness of the sheet material as measured at time of use is preferably from 2 to 15 in terms of ball tack. Specification, page 4, lines 3-4.

When the sheet material to be used has a tackiness of from 2 to 15 in terms of ball tack, this sheet material can be easily handled and, despite this, can be easily bonded provisionally to a semiconductor element. In addition, when this sheet material is press-bonded to the semiconductor element and substrate, a satisfactory adherent state is attained. Consequently, the semiconductor element can be encapsulated in a void-free state without fail. Specification, page 4, lines 7-15.

A preferred embodiment of the process for semiconductor device production of the invention described above comprises covering the back of the semiconductor element with the sheet material having an area larger than the back of the semiconductor element, press-bonding the sheet material to thereby coat the back and the edges of the semiconductor element with the sheet material, and then thermally curing the sheet material to thereby encapsulate the semiconductor element. Specification, page 4, lines 16-24.

According to this process, the back and the edges of the semiconductor element can be simultaneously sealed with the sheet material having an area larger than the back of the semiconductor element. In addition, upon press-bonding, the sheet material can conform to the

shape of the semiconductor element and encapsulate it without leaving a space between them. Specification, page 4, line 25 to page 5, line 5.

The present invention is defined by two independent claims on appeal, namely claims 1 and 2.

Claim 1 provides a semiconductor device which comprises a substrate and a semiconductor element mounted thereon through a bump bonding part, wherein the semiconductor element has been encapsulated by coating the back and the edges of the semiconductor element with a thermosetting sheet material having tackiness. Specification, page 3, lines 5-10 and page 5, lines 9-14.

Claim 2 provides a process for producing a semiconductor device which comprises a substrate and a semiconductor element mounted thereon through a bump bonding part, which comprises encapsulating the semiconductor element by coating the back and the edges of the semiconductor element with a thermosetting sheet material having tackiness. Specification, page 3, lines 16-22.

Claim 6 depends from claim 1 and recites that the thermosetting sheet material is a rubber-containing polycarbodiimide resin. Specification, page 5, lines 17-19.

Claim 7 depends from claim 1 and recites that the tackiness of the sheet material before thermosetting is 2 to 15 in terms of ball tack. Specification, page 4, lines 4-6.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1, 2 and 6 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Igarashi et al (U.S. Patent No. 5,990,546).

In the Final Action dated October 5, 2006, the Examiner asserts that Igarashi et al discloses in Figure 5(B), a semiconductor device that comprises a substrate 2 and a semiconductor element 1 mounted thereon through a bump bonding part (the ball pads shown in the Figure), wherein the semiconductor element has been encapsulated by coating the back and the edges of the semiconductor element with a thermosetting, rubber-containing sheet material having tackiness.

The Examiner considers the bonding agent that bonds the bonding sheet 33 to the chip to be a thermosetting sheet material. See Advisory Action mailed February 21, 2007, page 2.

Claim 7 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Igarashi et al.

The Examiner concedes that Igarashi et al does not explicitly disclose the tackiness of the sheet material as recited in the claim. However it is the Examiner's position that tackiness is a result effective variable and it would have been obvious for one of ordinary skill in the art to adjust the tackiness of the sheet material in terms of ball tack in accordance with the process for forming the sheet material, for the purpose of handling the package during or after the packaging process or testing the chip in the package.

VII. ARGUMENT

A. Claims 1, 2 and 6

The rejection of claims 1, 2 and 6 should be reversed since Igarashi et al does not disclose all elements of the claim.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Claim 1 of the present application is directed to a semiconductor device which comprises a substrate and a semiconductor element mounted thereon through a bump bonding part. Claim 1 further requires that the semiconductor element has been encapsulated by coating the back and the edges of the semiconductor element with a thermosetting sheet material having tackiness.

Claim 2 of the present application is directed to a process for producing a semiconductor device which comprises a substrate and a semiconductor element mounted thereon through a bump bonding part. The process comprises encapsulating the semiconductor element by coating the back and the edges of the semiconductor element with a thermosetting sheet material having tackiness.

The Examiner asserts that Igarashi et al discloses in Figure 5(B), a semiconductor device that comprises a substrate 2 and a semiconductor element 1 mounted thereon through a bump bonding part (the ball pads shown in the Figure), wherein the semiconductor element has been encapsulated by coating the back and the edges of the semiconductor element with a thermosetting, rubber-containing sheet material having tackiness.

The Examiner has previously asserted that element 33 of Igarashi et al is a thermosetting, rubber-containing sheet material (see Actions dated January 5, 2006 and April 25, 2006), and a bonding sheet by virtue of it being an epoxy resin in sheet form (see Action dated October 5, 2006).

As pointed out in the arguments presented in the Amendment filed on October 25, 2005 and the Response filed on April 5, 2006, Igarashi et al does not disclose, teach or suggest a "thermosetting sheet material" as recited in present claim 1. Specifically, as indicated in the Response filed April 5, 2006, the term "thermosetting" is used only at lines 27-28 of column 5 of Igarashi et al in the context of "a thermoplastic or thermosetting bonding *agent*". Thus, a sheet having a thermosetting property is not disclosed, taught or suggested by Igarashi et al. For at least this reason, the present invention is not anticipated by Igarashi et al.

Appellants have also previously pointed out that the material for the bonding sheet material in Figure 5(B) is not disclosed in the reference. That is, nowhere in Igarashi et al does it state that bonding sheet 33 is an epoxy resin. Therefore, the Examiner has not set forth a reasonable basis for asserting that the sheet material is rubber and inherently has at least some tackiness. As pointed out in the arguments presented in the Amendment filed on October 25, 2005, Igarashi et al teaches that the semiconductor chip is sealed by bonding a bonding sheet using an epoxy-rubber resin *as a bonding agent*. This does not mean that the bonding sheet itself is an epoxy rubber resin and therefore it does not follow that the bonding sheet contains rubber and necessarily has tackiness. Rather, the use of the epoxy-rubber resin as a bonding agent suggests to one of ordinary skill in the art that the bonding sheet itself does not have tackiness.

Further, there is no description in Igarashi et al which teaches or suggests that the bonding sheet itself contains rubber or has tackiness. Searching the full text of Igarashi et al, the term "rubber" is used only at lines 21 and 37 of column 7 within the context of "a bonding seat [sic] 33 (e.g., epoxy-rubber resin as bonding agent (emphasis added)". Thus, a sheet having rubber therein is not taught or suggested.

In addition to the above, Appellants have submitted an executed Declaration by Mr. Hideyuki Usui, one of the co-inventors named in Igarashi et al in support of the position that Igarashi et al does not teach an epoxy rubber bonding sheet as asserted by the Examiner. This Declaration is listed in the "Evidence Appendix" of the Brief and a copy is attached. Specifically, in the Declaration Mr. Usui confirms that the bonding sheet 33 of Igarashi et al uses an epoxy rubber resin as a bonding agent which makes it clear to one of ordinary skill in the art that the bonding sheet 33 of Igarashi et al does not itself contain a rubber and does not necessarily have tackiness as asserted by the Examiner. Additionally, Mr. Usui explains that there is a difference between the bonding agent of Igarashi et al and the bonding sheet of Igarashi et al.

Further, Mr. Usui confirms that there is no disclosure, teaching or suggestion of a thermosetting bonding sheet in Igarashi et al.

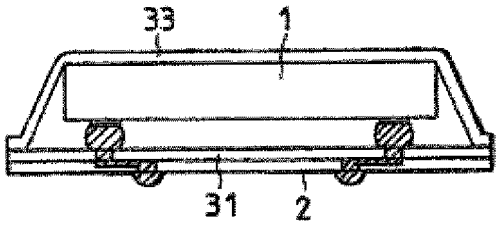
The Examiner now considers the bonding agent that bonds the bonding sheet 33 to the chip to be a thermosetting sheet material. See Advisory Action mailed February 21, 2007, page 2. Specifically, in the Advisory Action the Examiner states that element 33 in Igarashi, *per se*, was not intended by itself to be the thermosetting material, but the bonding agent that bonds it to

the chip is considered to be the thermosetting material. This current position taken by the Examiner is different from his previous position that "element 33 is a bonding sheet . . . by virtue of [it] being an epoxy resin in a sheet form . . ." in the Office Action dated October 5, 2006. See page 3, lines 4-5 of paragraph 6 under the heading "Response to Arguments". The Examiner has made other similar comments on the record, for example, in the Action dated January 5, 2006, regarding the disclosure of Igarashi, the Examiner stated, "the semiconductor element has been encapsulated by coating the back and the edges of the semiconductor element with a thermosetting, rubber containing *sheet material 33* having tackiness" (emphasis added).

However, contrary to the Examiner's new position, Igarashi et al does not disclose or teach that the "bonding agent" that bonds the sheet material 33 to the chip is a thermosetting "sheet" material and therefore, Igarashi et al does not disclose all elements of the present invention.

Figure 5(B) of Igarashi et al is reproduced below.

FIG. 5(B)



Referring to Fig 5(B), at column 7, lines 19-22, Igarashi states:

> . . .the transverse edge and back face of the semiconductor chip 1 are sealed by bonding of a bonding seat [sic] (e.g., for example using epoxy-rubber resin as bonding agent).

There is nothing in the disclosure of Igarashi et al that indicates that the bonding agent is a "sheet" material. Further, the Examiner has not set forth a reasonable basis for asserting that the bonding agent of Igarashi et al is a "sheet" material as required by present claim 1. Namely, it would not be reasonable to employ a second "sheet material" such as an epoxy-rubber resin as bonding agent between bonding sheet 33 and semiconductor chip 1 to bond the "sheet material 33" to the chip as suggested by the Examiner. For this additional reason, present claim 1 is not anticipated by Igarashi et al.

The present invention is characterized in that a thermosetting sheet material having tackiness is used. A sheet which does not have thermosetting properties cannot be used in the intended application (the field in which appropriate level of thermosetting property is required). Moreover, a mere thermosetting sheet having no tackiness does not exert the effects of the present invention. In view of the above, Igarashi et al does not disclose, teach or suggest a thermosetting sheet having tackiness as recited in present claim 1. Therefore, Igarashi et al does not disclose, teach or suggest at least two characteristics of the present invention and cannot be said to anticipate nor render obvious the present claims.

Claims 2 and 6 includes the same distinguishing recitations as claim 1 and are distinguished over the art for at least the same reasons as claim 1. Further, Igarashi et al does not specifically disclose a rubber-containing or rubber-modified polycarbodiimide resin and therefore claim 6 is not anticipated nor rendered obvious by the art of record.

Appellants respectfully submit that the Examiner must consider the totality of the evidence provided on the record, which establishes that Igarashi et al does not disclose, teach or

suggest a thermosetting bonding sheet having tackiness as recited in claim 1. The ultimate determination of patentability is based on the entire record, by a preponderance of evidence, with due consideration to the persuasiveness of any arguments and any secondary evidence. See MPEP § 2142 citing *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). The legal standard of "a preponderance of evidence" requires the evidence to be more convincing than the evidence which is offered in opposition to it. When an Applicant submits evidence, whether in the specification as originally filed or in reply to a rejection, the Examiner must reconsider the patentability of the claimed invention and the decision on patentability must be made based upon consideration of all the evidence, including the evidence submitted by the Examiner and the evidence submitted by the Applicant. A decision to make or maintain a rejection in the face of all the evidence must show that it was based on the totality of the evidence. Facts established by rebuttal evidence must be evaluated along with the facts on which the conclusion was reached, not against the conclusion itself. See MPEP § 2142 citing *In re Eli Lilly & Co.*, 902 F.2d 943, 14 USPQ2d 1741 (Fed. Cir. 1990).

In this case, the Examiner has made statements regarding the disclosure of Igarashi et al which are contradicted by objective evidence of the teachings of Igarashi et al itself as well as the knowledge and skill available in the art and the Declaration of Mr. Usui submitted herewith. The Examiner has not offered any factual evidence in support of his position that the bonding agent of Igarashi et al is a thermosetting sheet material. Accordingly, the evidence presented by Appellants is more convincing than the mere statements of the Examiner which are not based on the actual disclosure of the reference. Therefore, patentability of the present claims is supported

by a preponderance of the evidence when the totality of the record is properly taken into consideration.

Accordingly, Appellants respectfully submit that the anticipation rejection should be reversed.

B. Claim 7

The rejection of claim 7 should be reversed because Igarashi et al does not teach or suggest the present invention.

Igarashi et al does not disclose, teach or suggest a thermosetting sheet material having tackiness as recited in present claim 1 from which claim 7 depends. Therefore, for at least this reason claim 7 is distinguished over the art of record.

Additionally, since Igarashi et al does not teach or suggest a thermosetting sheet material having tackiness, there is no motivation for one of ordinary skill in the art to modify the disclosure of Igarashi et al to arrive at the tackiness of the sheet material before thermosetting of 2 to 15 in terms of ball tack as recited in present claim 7. For this additional reason, claim 7 is distinguished over Igarashi et al.

Accordingly, Appellants respectfully submit that the obviousness rejection should be reversed.

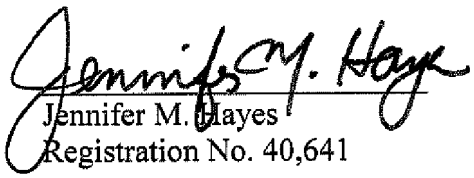
VII. Conclusion

The fee required under 37 C.F.R. §41.37(a) and 1.17(c) is being charged to Deposit Account No. 19-4880 via EFS Payment screen.

Unless a check is submitted herewith for the fee required under 37 C.F.R. §41.37(a) and 1.17(c), please charge said fee to Deposit Account No. 19-4880.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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Date: April 25, 2007

CLAIMS APPENDIX

CLAIMS 1, 2, 6 and 7 ON APPEAL:

1. A semiconductor device which comprises a substrate and a semiconductor element mounted thereon through a bump bonding part, wherein

the semiconductor element has been encapsulated by coating the back and the edges of the semiconductor element with a thermosetting sheet material having tackiness.

2. A process for producing a semiconductor device which comprises a substrate and a semiconductor element mounted thereon through a bump bonding part, which comprises encapsulating the semiconductor element by coating the back and the edges of the semiconductor element with a thermosetting sheet material having tackiness.

6. The semiconductor device of claim 1, wherein the thermosetting sheet material is a rubber-containing or rubber-modified polycarbodiimide resin.

7. The semiconductor device of claim 1, wherein the tackiness of the sheet material before thermosetting is 2 to 15 in terms of ball tack.

EVIDENCE APPENDIX:

Pursuant to 37 C.F.R. § 41.37(c)(1)(ix), submitted herewith are copies of any evidence submitted pursuant to 37 C.F.R. §§ 1.130, 1.131, or 1.132 or any other evidence entered by the Examiner and relied upon by Appellant in the appeal.

The attached Declaration under 37 C.F.R. § 1.132 of Mr. Hideyuki Usui was submitted on January 5, 2007.

RELATED PROCEEDINGS APPENDIX

Submitted herewith are copies of decisions rendered by a court or the Board in any proceeding identified about in Section II pursuant to 37 C.F.R. § 41.37(c)(1)(ii).

None

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SUBMISSION OF APPEAL BRIEF

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith please find an Appeal Brief. The statutory fee of $500.00 is being charged to Deposit Account No. 19-4880 via EFS Payment Screen. The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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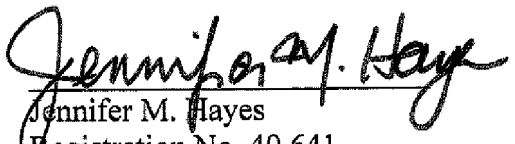

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